SH69P25

OTP 4K 4-Bit Micro-controller

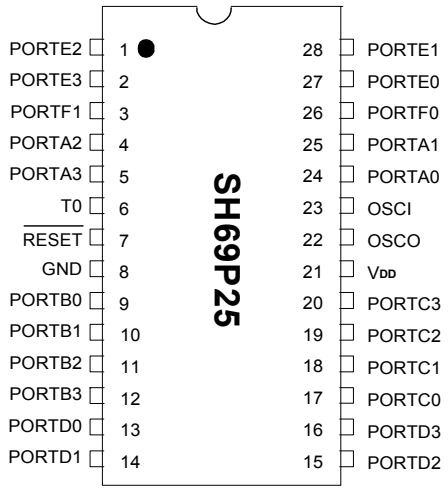
Features

- SH6610C-Based Single-Chip 4-Bit Micro-Controller
- OTPROM: 4K X 16 bits
- RAM: 160 X 4 bits (data memory)
- Operation Voltage: 2.4V - 5.5V (Typical 5.0V)
- 22 CMOS Bi-directional I/O Pins
- Built-in Pull-high and Pull-low Resistor for PortA - PortF
- 4-Level Subroutine Nesting (including interrupts)
- One 8-Bit Auto Re-load Timer/Counter
- Warm-Up timer
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - External Interrupts: PORTB & PORTC (rising/falling edge)
- Oscillator (OTP option)
  - Crystal Oscillator: 32.768k - 4MHz
  - Ceramic Resonator: 400k - 4MHz
  - RC Oscillator: 400k - 4MHz
  - External Clock: 30k - 4MHz
- Instruction cycle time:
  - 4/32.768kHz (122μs) for 32.768kHz OSC clock
  - 4/4MHz (1μs) for 4MHz OSC clock
- Two Low Power Operation Modes: HALT and STOP
- Reset
  - Built-in Watch Dog Timer (WDT) (OTP option)
  - Built-in Power On Reset (POR)
  - Built-in Low Voltage Reset (LVR)
- Two LVR Level (OTP option)
  - Level 1: 2.5V
  - Level 2: 4.0V
- OTP type & Code protection

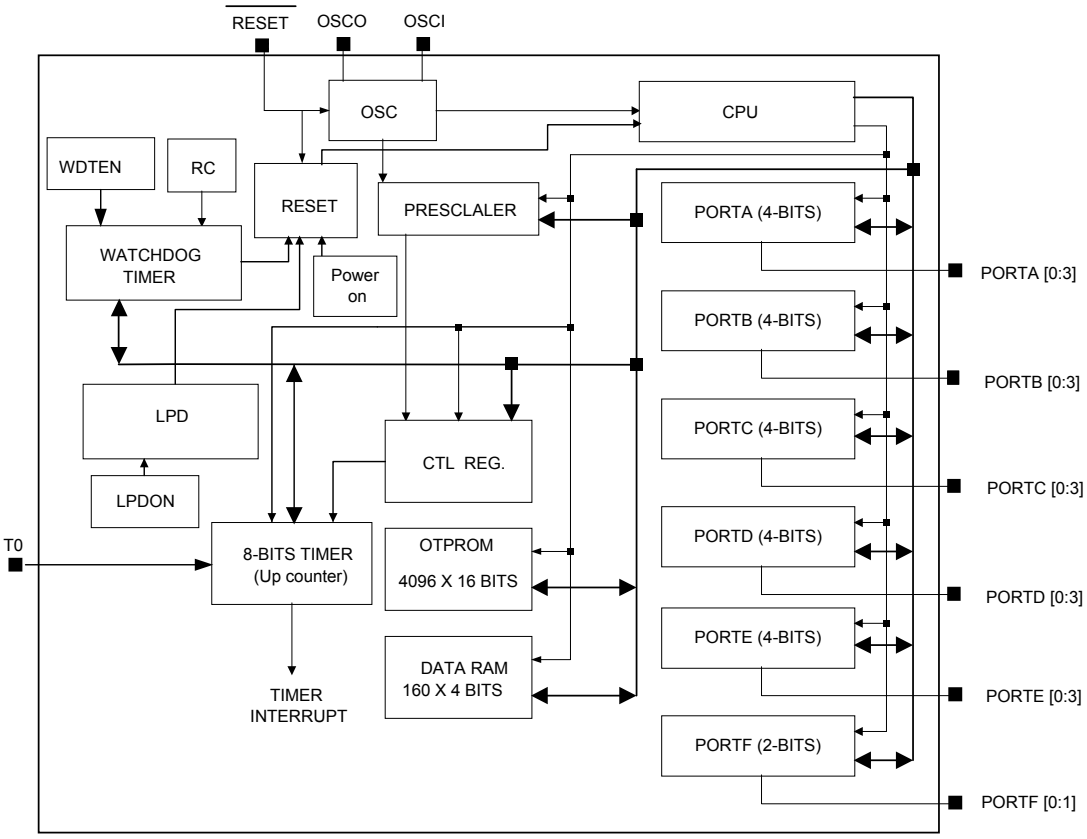
General Description

The SH69P25 is a 4-bit micro-controller. This chip integrates the SH6610C 4-bit CPU core with SRAM, 4K OTPROM, Timer and I/O Ports.

Pin Configuration



Block Diagram



Pin Description (Normal Mode)

Pin No.	Designation	I/O	Descriptions
27, 28, 1, 2	PORTE [0:3]	I/O	Bit programmable I/O
26, 3	PORTF [0:1]	I/O	Bit programmable I/O
24, 25, 4, 5	PORTA [0:3]	I/O	Bit programmable I/O
6	T0	I	Timer Clock/Counter input pin. (Schmitt trigger input)
7	$\overline{\text{RESET}}$	I	Reset input (active low, Schmitt trigger input)
8	GND	P	Ground pin
9 - 12	PORTB [0:3]	I/O	Bit programmable I/O Vector Interrupt (Active rising or falling edge by system register setup)
13 - 16	PORTD [0:3]	I/O	Bit programmable I/O
17 - 20	PORTC [0:3]	I/O	Bit programmable I/O Vector Interrupt (Active rising or falling edge by system register setup)
21	V_{DD}	P	Power supply pin
22	OSCO	O	OSC output pin. No output in RC mode
23	OSCI	I	OSC input pin, connected to a crystal, ceramic or external resistor

OTP Programming Pin Description (OTP Program Mode)

Pin No.	Symbol	I/O	Shared by	Description
21	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
7	V_{PP}	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
8	GND	P	GND	Ground
23	SCK	I	OSCI	Programming Clock input pin
24	SDA	I/O	PORTA0	Programming Data pin

Function Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 4K program ROM. It consists of 12-bits: the Page Register (PC11), and the Ripple Carry Counters (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, and PC0).

The program counter normally increases by one (+1) for every execution of an instruction except for the following cases:

(1) When executing a jump instruction (such as JMP, BA0),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and retrieved back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (AC) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

1.6. Stack

A group of registers are used to save the contents of CY & PC (11-0) sequentially for each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

Note:

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on the first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupt requests. Note that a program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of the stack will be shifted out.

2. OTP ROM

The SH69P25 can address up to 4K X 16bits words of the program area from $000 to $FFF.
Service routine serves as the starting vector address.

Address	Instruction	Remarks
$000H	JMP Instruction	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP Instruction	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP Instruction	Jump to PBC service routine

3. RAM

The built-in RAM consists of general-purpose data memories and system registers. Direct addressing in one instruction can access both data memory and system register.

The memory allocation map is shown below:

$000 - $01F: System register and I/O
$020 - $0BF: Data memory (160 X 4 bits, divided into 2 banks. $020 - $07F: bank0, $080 - $0BF: bank1)

3.1. The Configuration of the System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06 - $07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	-	-	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13 - $14	-	-	-	-	-	Reserved
$15	PULLEN	PH/PL	PBCFR	-	R/W	Bit1: PBC interrupt rising / failing edge set Bit2: PORT Pull-high/low set Bit3: PORT Pull-high/low enable control
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	PORTA input/output control
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	PORTB input/output control
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	PORTC input/output control
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	R/W	PORTD input/output control
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	R/W	PORTE input/output control
$1B	-	-	PF1OUT	PF0OUT	R/W	PORTF input/output control
$1C	-	-	T0S	T0E	R/W	Bit0: T0 signal edge; Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	WDT	-	-	-	W	Bit3: WDT timer reset (write 1 to reset WDT)
$1F	-	-	-	-	-	Reserved

* System Register $0E - $12 refer to "SH6610C User manual".

3.2. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	-	IET0	-	IEP	- 0 - 0	- 0 - 0
$01	-	IRQT0	-	IRQP	- 0 - 0	- 0 - 0
$02	-	TM0.2	TM0.1	TM0.0	- 000	- 000
$03	-	-	-	-	-	-
$04	TL0.3	TL0.2	TL0.1	TL0.0	0000	0000
$05	TH0.3	TH0.2	TH0.1	TH0.0	0000	0000
$06 - $07	-	-	-	-	-	-
$08	PA.3	PA.2	PA.1	PA.0	1111	1111
$09	PB.3	PB.2	PB.1	PB.0	1111	1111
$0A	PC.3	PC.2	PC.1	PC.0	1111	1111
$0B	PD.3	PD.2	PD.1	PD.0	1111	1111
$0C	PE.3	PE.2	PE.1	PE.0	1111	1111
$0D	-	-	PF.1	PF.0	- -11	- -11
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13 - $14	-	-	-	-	-	-
$15	PULLEN	PH/PL	PBCFR	-	010 -	010 -
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	0000	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	0000	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0000	0000
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	0000	0000
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	0000	0000
$1B	-	-	PF1OUT	PF0OUT	- - 00	- - 00
$1C	-	-	T0S	T0E	- - 00	- - 00
$1D	-	-	-	-	-	-
$1E	WDT	-	-	-	-	-
$1F	-	-	-	-	-	-

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

3.3. Others Initial State:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

4. System Clock and Oscillator

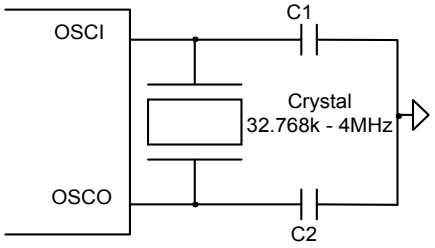
System clock generator produces the basic clock pulses that provide the system clock to the CPU and any peripherals.
Instruction cycle time

(1) 4/32.768kHz (122μs) for 32.768kHz Oscillator

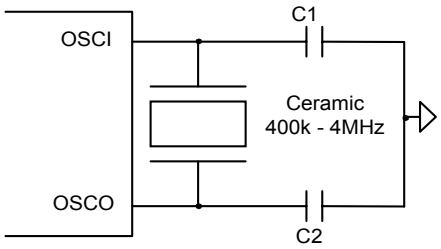
(2) 4/4MHz (1μs) for 4MHz Oscillator

4.1. Oscillator Type

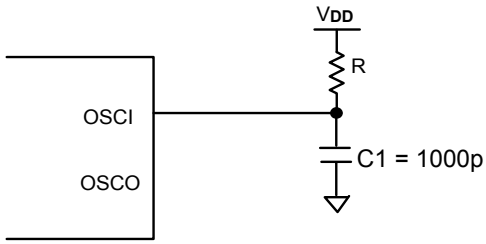
(1) Crystal oscillator: 32.768kHz - 4MHz.



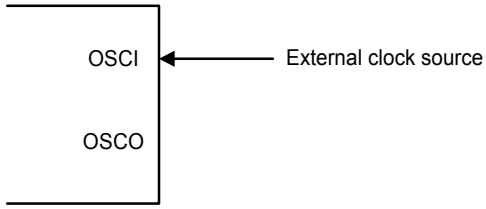
(2) Ceramic resonator: 400kHz - 4MHz.



(3) RC oscillator: 400kHz - 4MHz.



(4) External input clock: 30kHz - 4MHz.

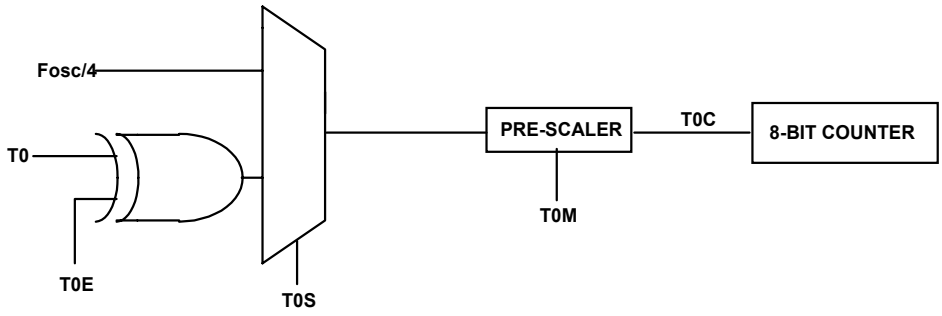


5. Timer0

SH69P25 has one 8-bit timer. The time/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The simplified timer block diagram is shown below:



5.1. Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Both counter and load register have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter. Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is loaded with the contents of the load register automatically when the high order digit is written or the counter counts overflow from $FF to $00.

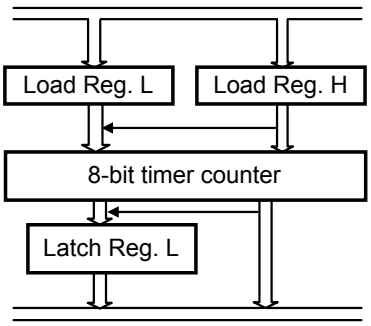
Timer Load Register: Since the register H controls the physical READ and WRITE operation, please follow these rules:

Write Operation:

First write Low nibble,
Then write High nibble to update the counter.

Read Operation:

High nibble first;
Followed by Low nibble.



5.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to waken the CPU from the HALT mode.

5.3. Timer0 Mode Register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0). The 8-bit counter counts prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in table1. These mode registers select the input pulse sources into the timer.

Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

5.4. External Clock/Event T0 as Timer0 Source

When an external clock/event input is used for the TM0, it is synchronized with the CPU system clock. Therefore the external source must follow certain constraints. The output from the T0M multiplex is T0C. It is sampled by the system clock in instruction frame cycle. Therefore it is necessary for the T0C to be high (at least 2 t**osc**) and low (at least 2 t**osc**). When the prescaler ratio is set to $/2^0$, the T0C is the same as the system clock input. Therefore the requirements are as follows

T0H = T0CH = T0 high time $\geq$ 2 t**osc** + ΔT

T0L = T0CL = T0 low time $\geq$ 2 t**osc** + ΔT

Note: ΔT = 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical.

Then:

$$\text{T0C high time} = \text{T0C low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = prescaler value

The requirement is, therefore:

$$\frac{N * T0}{2} \geq 2\ t\mathbf{osc} + \Delta T \text{ , or } T0 \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

The limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

System Register $1C

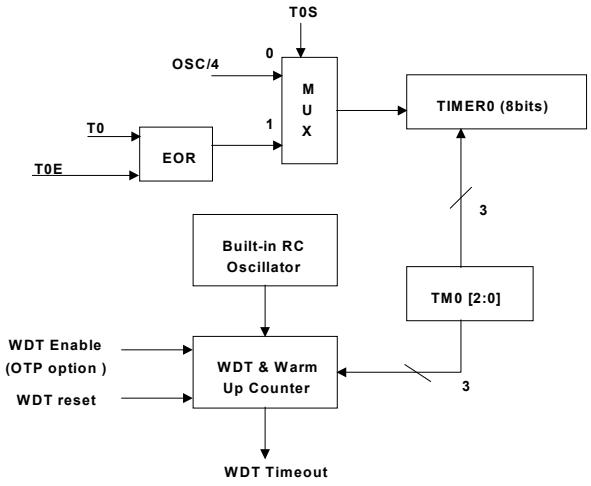
Address	BIT3	BIT2	BIT1	BIT0	R/W	Remark
$1C	-	-	T0S	T0E	R/W	Bit0: T0 signal edge Bit1: T0 signal source

T0E: T0 signal edge

0: Increment on low-to-high transition T0 pin (Power on initial)
1: Increment on high-to-low transition T0 pin

T0S: T0 signal source

0: OSC/4 (Power on initial)
1: Transition on T0 pin



6. I/O Ports

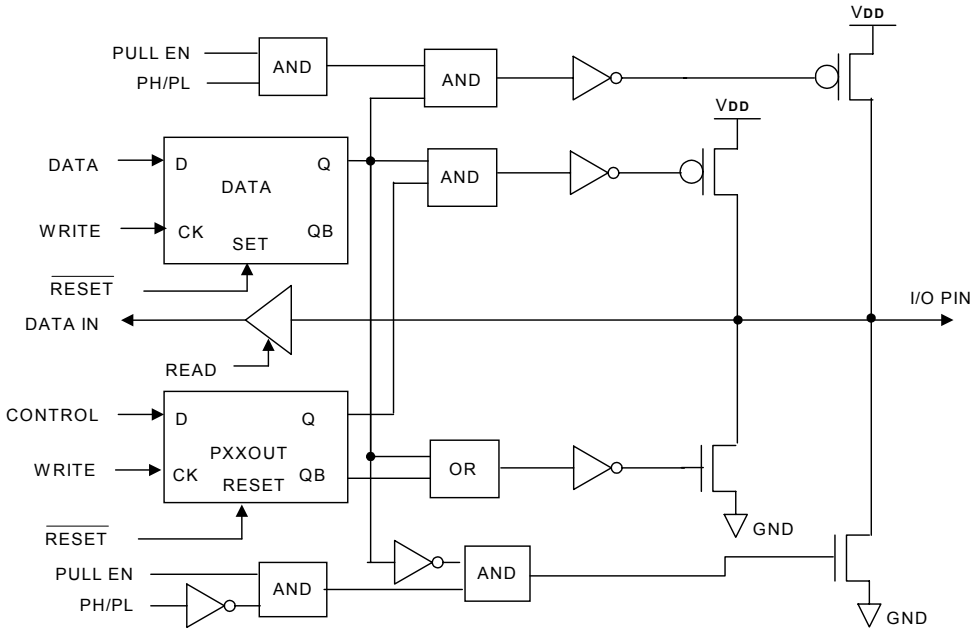
The SH69P25 provides 22 I/O pins. The port control register controls ON/OFF of the output buffer. The following sections show the circuit configuration of I/O ports.

Every I/O pin has an internal pull high / pull low resistor, which is controlled by PULLEN and PH/PL of $15.

Each of these ports contains 4 or 2(PF) bits I/O pins. ON/OFF of the output buffer for the port can be controlled by the port control register. Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	1111
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	1111
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	1111
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD	1111
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE	1111
$0D	-	-	PF.1	PF.0	R/W	PORTF	- -11

Equivalent Circuit for a Single I/O Pin



System Register $15 - $1B

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$15	PULLEN	PH/PL	PBCFR	-	R/W	Bit1: PBC interrupt rising / failing edge set Bit2: PORT Pull-high/low set Bit3: PORT Pull-high/low enable control	010 -
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	PORTA input/output control	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	PORTB input/output control	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	PORTC input/output control	0000
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	R/W	PORTD input/output control	0000
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	R/W	PORTE input/output control	0000
$1B	-	-	PF1OUT	PF0OUT	R/W	PORTF input/output control	- - 00

PAXOUT, PBXOUT, PCXOUT, PDXOUT, PEXOUT (X = 0, 1, 2, 3), PFXOUT (X = 0, 1)

1: Used as an output buffer

0: Used as an input buffer (Power on initial)

PBCFR: 1: Rising Edge interrupt, 0: Falling Edge interrupt,
PH/PL: 1: Port Pull high resistor ON, 0: Port Pull low resistor ON,
PULLEN: 1: Port Pull high /Pull low enable, 0: Port Pull high /Pull low disable

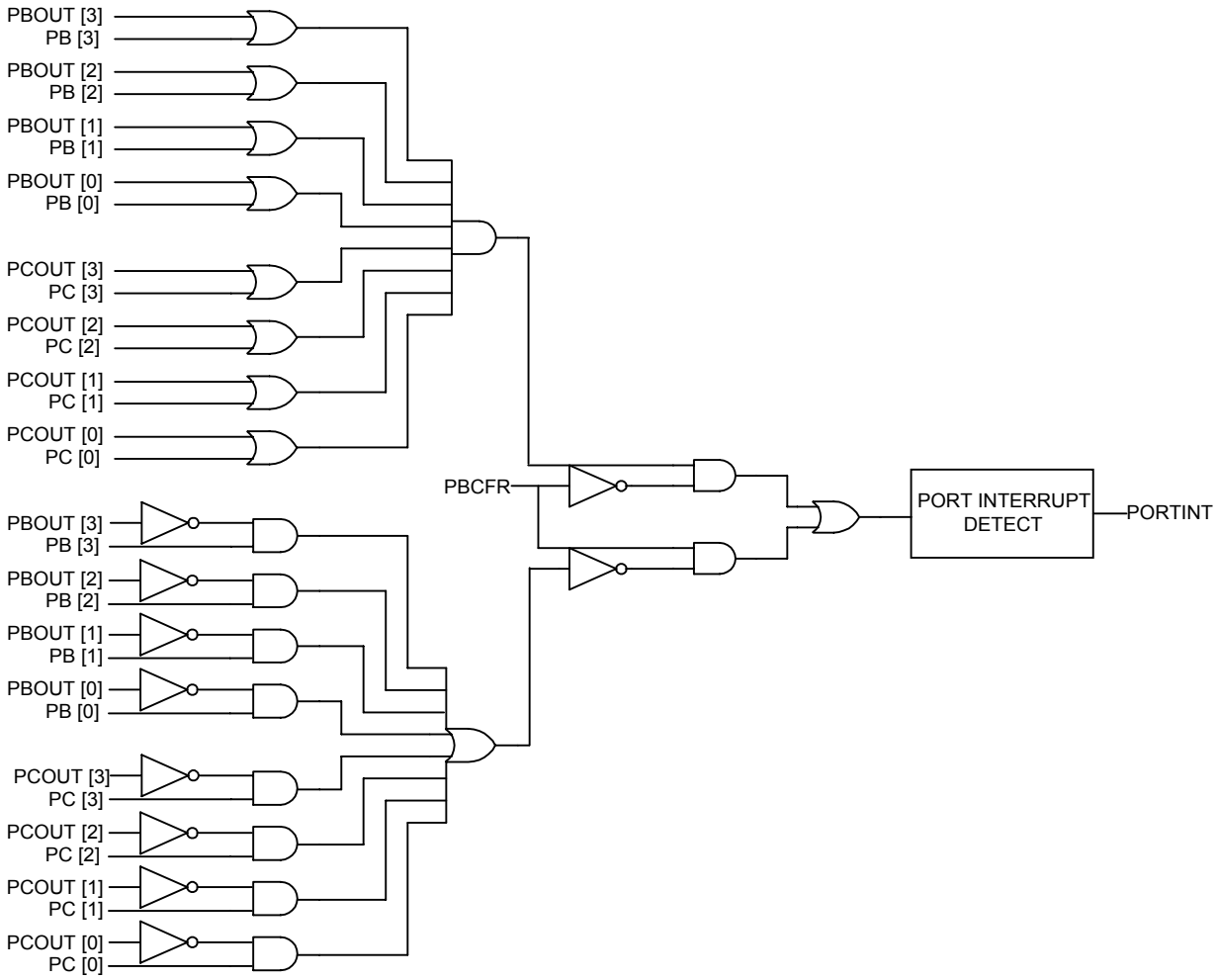
PORTB & PORTC Interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, so only the input port can generate an external interrupt.

When PBCFR is set to 0, any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD}.

When PBCFR is set to 1, any one of the PORTB and PORTC input pin transitions from GND to V_{DD} will generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.

The port interrupt function block-diagram is shown below.



7.Interrupt

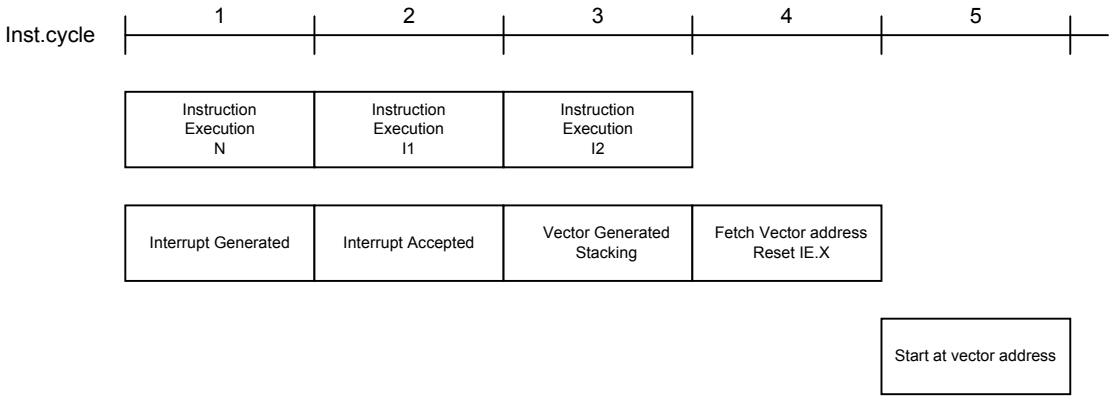
Two interrupt sources are available on SH69P25:
- Timer0 interrupt
- Port B - C interrupts (Falling/Rising edge)

7.1. Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

8. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by OTP option.

The LVR circuit has the following functions:

- It generates an internal reset signal when $V_{DD} \leq V_{LVR}$
- It cancels the internal reset signal when $V_{DD} > V_{LVR}$

Here, V_{DD}: power supply voltage, V_{LVR}: LVR detect voltage, There are two levels selected by OTP option:
Level 1: 2.3 - 2.7V, typical 2.5V
Level 2: 3.8 - 4.2V, typical 4.0V

LVR can be enabled or disabled permanently by OTP option.

9. Watch Dog Timer (WDT)

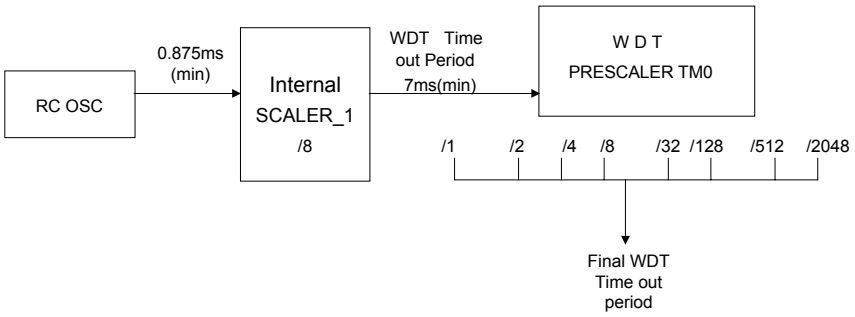
System Register $1E

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset. (write 1 to reset WDT)

The input clock of the watchdog timer is generated by a built-in RC oscillator so that the WDT will always run even in the STOP mode. SH69P25 generates a RESET condition when the watchdog times-out. The watchdog can be enabled or disabled permanently by using the OTP option. To prevent its timing out and generating a device RESET condition, you should write this bit as “1” before timing-out. The WDT has a time-out period of more than 7ms (typical 18ms). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controlled by writing to the TM0 register.

Pre-scaler divide ratio:

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Timer-out Period
1	1	1	1: 1	7ms
1	1	0	1: 2	14ms
1	0	1	1: 4	28ms
1	0	0	1: 8	56ms
0	1	1	1: 32	224ms
0	1	0	1: 128	896ms
0	0	1	1: 512	3,584ms
0	0	0	1: 2048 (Power on initial)	14,336ms



10. HALT and STOP Mode

After the execution of HALT instruction, the device will enter halt mode. In the halt mode, CPU will stop operating. But peripheral circuit (Timer0) will keep operating.

After the execution of STOP instruction, the device will enter stop mode. In the stop mode, the whole chip (including oscillator) will stop operating without watchdog timer, if it is enabled.

In HALT mode, SH69P25 can be waked up if any interrupt occurs.

In STOP mode, SH69P25 can be waked up if port interrupt occurs or watchdog timer overflow (WDT is enabled).

11. OTP Option

11.1. Oscillator:

External Clock: System Clock is provided by External Clock through OSCI
RC Osc: System Clock is provided by External RC through OSCI
Crystal/Ceremic Resonator 400k - 4M: System Clock is provided by Crystal/Ceremic Resonator through OSCI and OSCO
X'tal (32768): System Clock is provided by Crystal (32.768k) through OSCI and OSCO

11.2. Watchdog Timer

Enable: Enable the watchdog timer
Disable: Disable the watchdog timer

11.3. LVR

Off: Disable the LVR function
On: Enable the LVR function

11.4. LVR Voltage

4V: Generate an internal reset signal when $V_{DD} \leq 4V$, if LVR enable
2.5V: Generate an internal reset signal when $V_{DD} \leq 2.5V$, if LVR enable

11.5. Osc

32k - 2M: The Oscillator frequency is between 32768Hz and 2MHz
2M - 4M: The Oscillator frequency is between 2MHz and 4MHz

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instructions

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instructions

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not including p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Including p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank Every $7F as one RAM bank
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . . .-0.3V to +7.0V

Input/Output Voltage . . . . . GND - 0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . .-40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	
Operating Current	I_{OP}	-	0.6	1.0	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	0.5	mA	All output pins unloaded
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded, LVR off (If LVR on, I_{SB2X} = I_{SB2} + 2μA) WDT off (If WDT on, I_{SB2X} = I_{SB2} + 20μA)
Input Low Voltage	V_{IL1}	GND	-	0.2 X V_{DD}	V	I/O ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0
Input Low Voltage	V_{IL3}	GND	-	0.15 X V_{DD}	V	OSCI (Driven by external clock)
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD}	V	I/O ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}	-	V_{DD}	V	OSCI (Driven by external Clock)
Input Leakage Current	I_{IL1}	-1	-	1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5	-	-	μA	$V_{\overline{\text{RESET}}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}	-	1	5	μA	$V_{\overline{\text{RESET}}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{T0} < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Pull-high/Pull-low Resistor	R_P	-	150	-	kΩ	PULL-HIGH/PULL-LOW resistor
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -10mA
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O ports, I_{OL} = 20mA

AC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T_{OSC1}	-	-	1	s	X'tal osc = 32.768kHz
RESET pulse width (low)	T_{RESET}	10	-	-	μs	V_{DD} = 5.0V
WDT Period	T_{WDT}	7	18	-	ms	V_{DD} = 5.0V
Frequency Stability (RC)	Δ F/F	-	-	20	%	RC Oscillator: |F (5.0V) - F (4.5V)|/F (5.0V)

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	4.5	V	
Operating Current	I_{OP}	-	0.3	0.6	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	0.2	mA	All output pins unloaded
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded, LVR off (If LVR on, I_{SB2X} = I_{SB2} + 2μA) WDT off (If WDT on, I_{SB2X} = I_{SB2} + 20μA)
Input Low Voltage	V_{IL1}	GND	-	0.2 X V_{DD}	V	I/O ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0
Input Low Voltage	V_{IL3}	GND	-	0.15 X V_{DD}	V	OSCI (Driven by external clock)
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD}	V	I/O ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}	-	V_{DD}	V	OSCI (Driven by external Clock)
Input Leakage Current	I_{IL1}	-1	-	1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5	-	-	μA	$V_{\overline{\text{RESET}}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}	-	1	5	μA	$V_{\overline{\text{RESET}}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{T0} < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -7mA, V_{DD} = 3V
Output Low Voltage	V_{OL}	-	-	GND + 0.4	V	I/O ports, I_{OL} = 8mA, V_{DD} = 3V

User Notice:
Max. Current into V_{DD} = 100mA
Max. Current out of GND = 150mA
Max. Output current sunk by any I/O port = 50mA
Max. Output current sourced by any I/O port = 40mA

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T_{OSC1}	-	-	1	s	Crystal Osc = 32.768kHz, V_{DD} = 3.0V
RESET pulse width (low)	T_{RESET}	12	-	-	μs	V_{DD} = 3.0V
WDT Period	T_{WDT}	7	18	-	ms	V_{DD} = 3.0V
Frequency Stability (RC)	Δ F/F	-	-	20	%	RC oscillator (1MHz): |F (3.0V) - F (2.7V)|/F (3.0V)

Low Voltage Reset Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified.

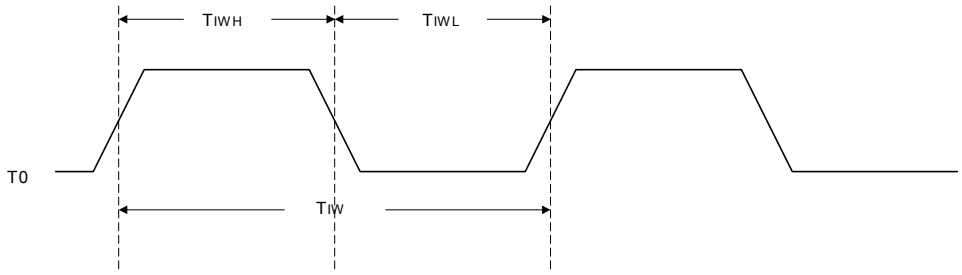
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage 1	V_{LVR1}	2.3	2.5	2.7	V	LVR enable
LVR Voltage 2	V_{LVR2}	3.8	4.0	4.2	V	LVR enable

AC Characteristics

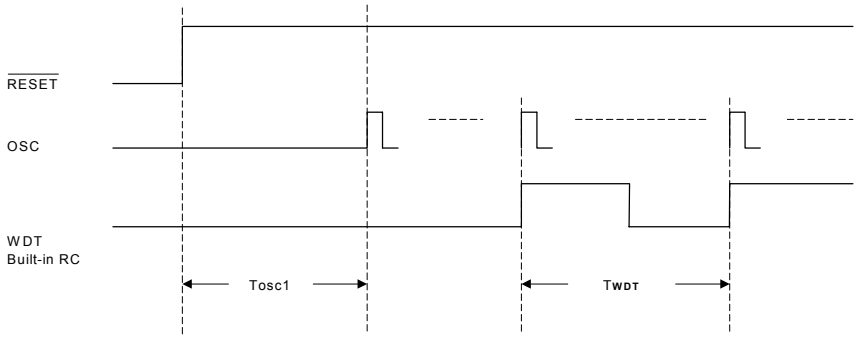
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CY}	Instruction Cycle Time	1	-	122	μs	
T_{IW}	T0 Input Width	(T_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
T_{IWH}	High Pulse Width	1/2 T_{IW}	-	-	ns	
T_{IWL}	Low Pulse Width	1/2 T_{IW}	-	-	ns	

Timing Waveform

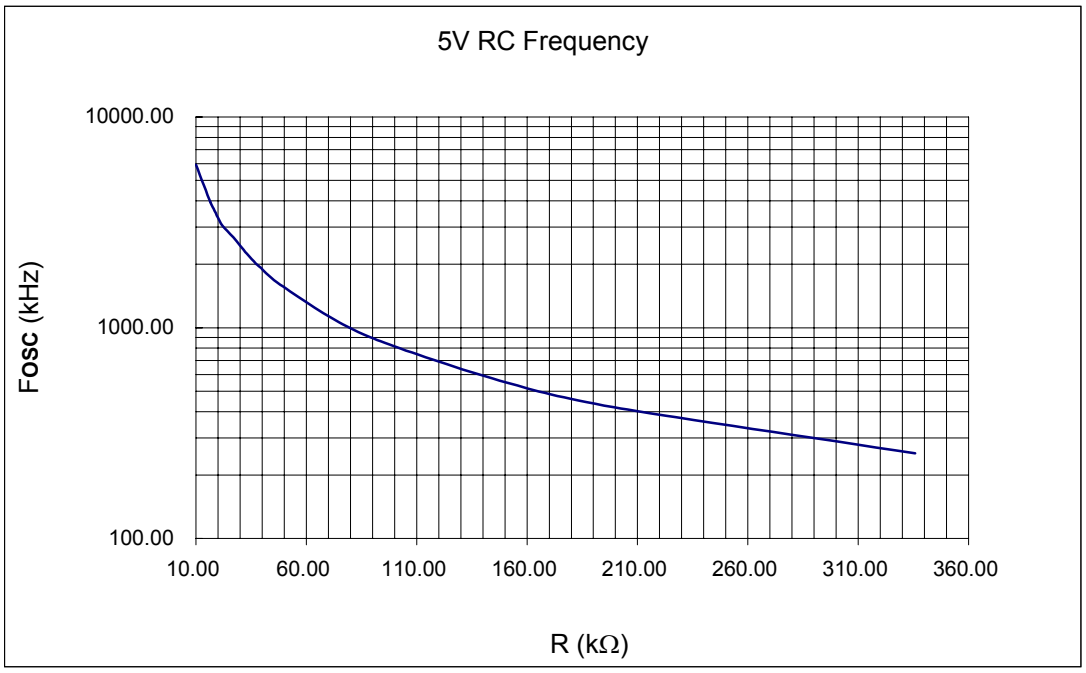
T0 Input Waveform



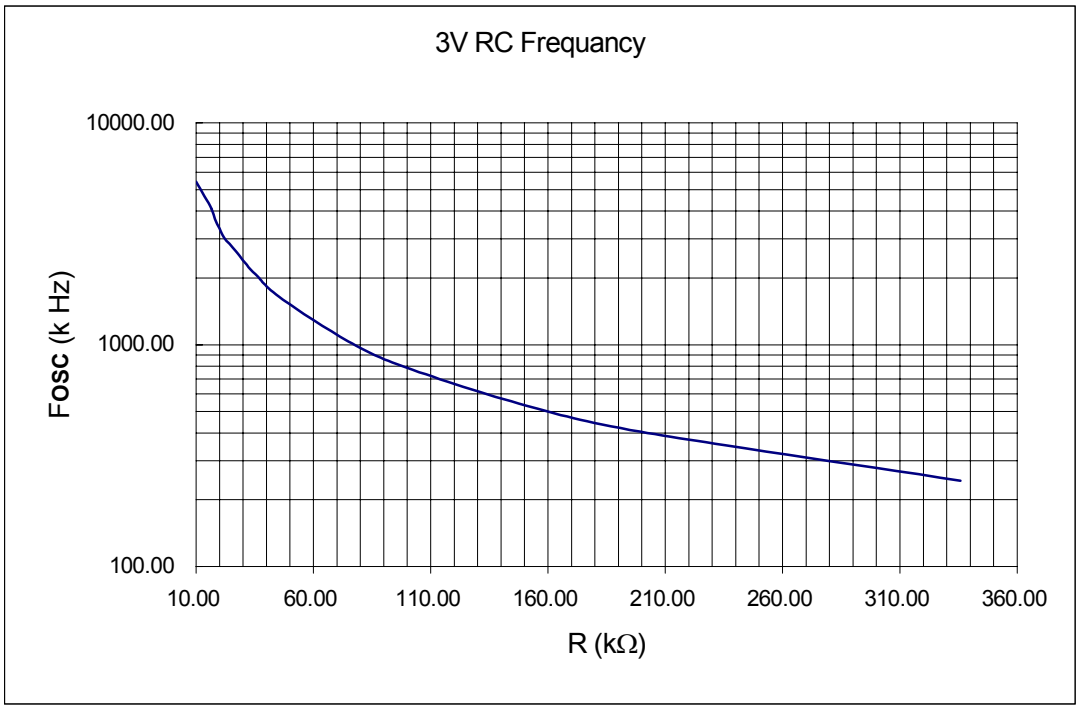
Built-in RC Oscillator (Only use for Watch Dog)



Typical RC Oscillator Resistor vs. Frequency: (V_{DD} = 5V, for reference only)



Typical RC Oscillator Resistor vs. Frequency: (V_{DD} = 3V, for reference only)

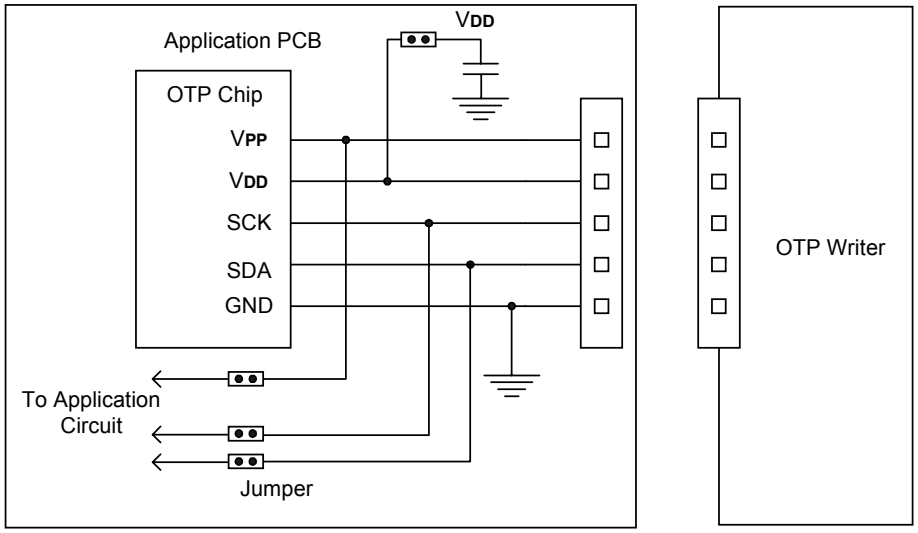


In System Programming Notice for OTP

The In System Programming technology is valid for SinoWealth OTP chip.

The Programming Interface of the OTP chip must be set on the user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended step is as follow for these jumpers:

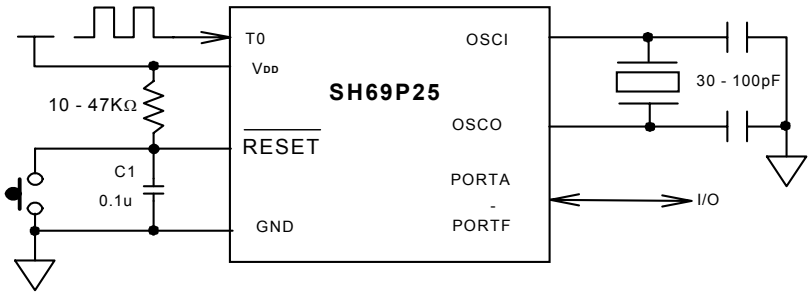
(1) The jumper is Open to separate the programming pins from the application circuit before programming the code.
(2) Connect the programming interface with OTP Writer and Begin Programming code.
(3) Disconnect OTP writer and short these jumpers when programming is finished.

For more detail information, please refer to the OTP writer user manual.

Application Circuit (for reference only)

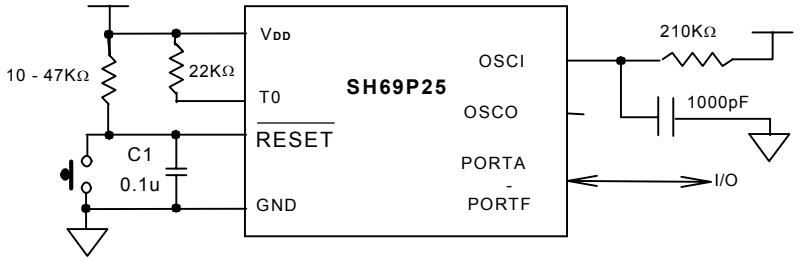
AP1

(1) Operating voltage: 5.0V
(2) Oscillator: Ceramic resonator 400kHz
(3) T0 input timer clock / counter
(4) PORTA - F: I/O



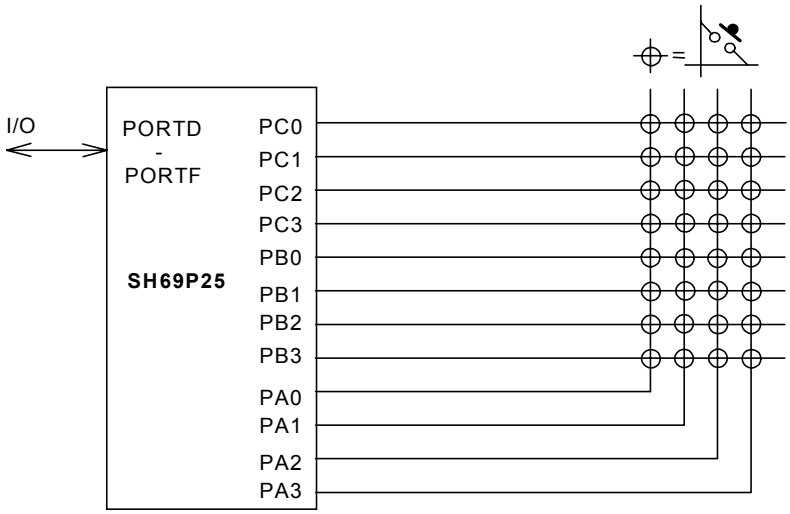
AP2

(1) Operating voltage: 5.0V
(2) Oscillator: RC 400kHz
(3) PORTA - F: I/O



AP3

(1) PORTA - C: as scan KEY BOARD (32 keys)
(2) PORTD - F: I/O,
(3) All input pins internal Pull high On



AP4 (Weight Scale)

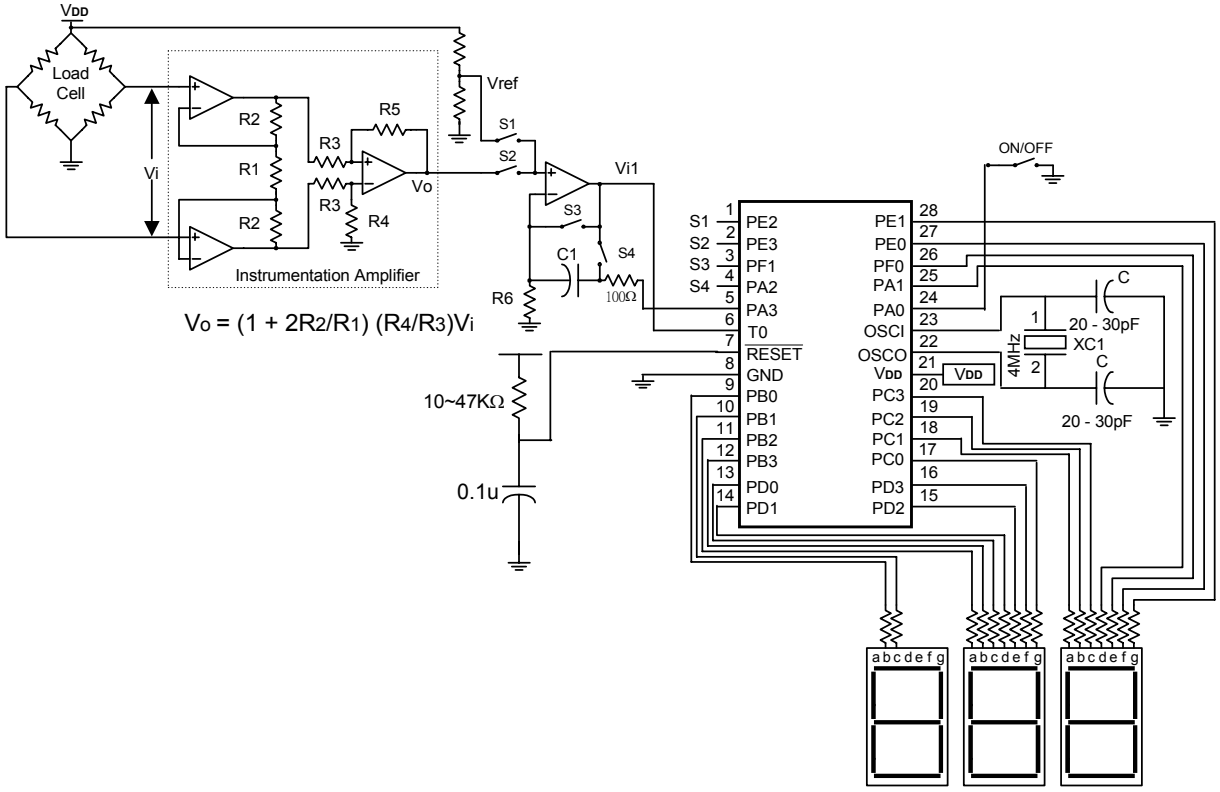
(1) Operating voltage: 5.0V

(2) Oscillator: Ceramic resonator 4MHz

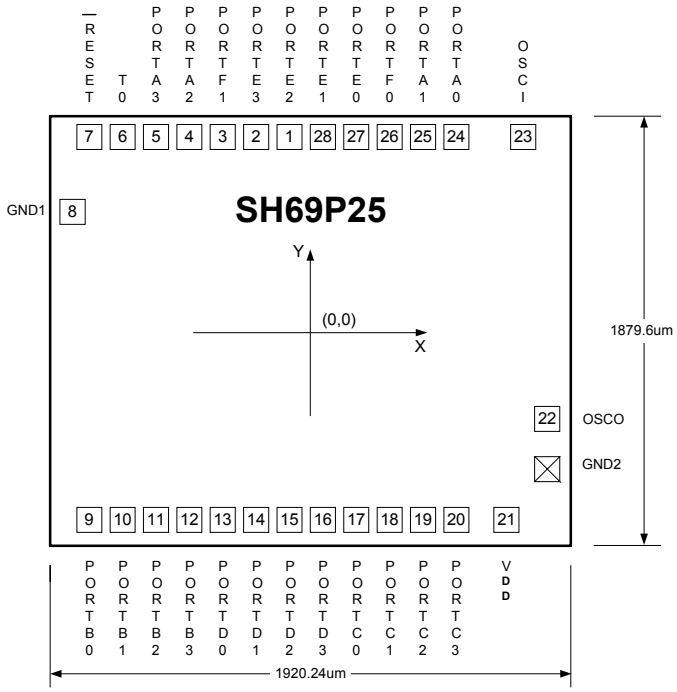
(3) Port A0: External interrupt input for ON/OFF switch

(4) Port E2, E3, F1, A2: S1 - S4 analog switch control signals that control Vi1 are charged or discharged by both reference voltage (Vref) and amplified voltage (Vo). The charging and discharging times are determined by the values of C1, R4 and the threshold voltage of the T0 input pin and the ADC resolution can be up to 8 bits

(5) Other Ports: Sink seven-segment LED current directly. 0 - 199 can be displayed in this configuration



Bonding Diagram



Note:

1. GND1 bonding to ground
2. GND2 bonding to Substratum
3. Substratum connects to ground

Pad Location

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTE 2	-23	749.5	16	PORTD 3	114	-749.5
2	PORTE 3	-153	749.5	17	PORTC 0	244	-749.5
3	PORTF 1	-283	749.5	18	PORTC 1	374	-749.5
4	PORTA 2	-413	749.5	19	PORTC 2	504	-749.5
5	PORTA 3	-543	749.5	20	PORTC 3	634	-749.5
6	T0	-673	749.5	21	V_{DD}	769	-749.5
7	$\overline{\text{RESET}}$	-803	749.5		GND2	822	-619.5
8	GND1	-818	585	22	OSCO	725	-420
9	PORTB 0	-796	-749.5	23	OSCI	767	749.5
10	PORTB 1	-666	-749.5	24	PORTA 0	587	749.5
11	PORTB 2	-536	-749.5	25	PORTA 1	467	749.5
12	PORTB 3	-406	-749.5	26	PORTF 0	347	749.5
13	PORTD 0	-276	-749.5	27	PORTE 0	227	749.5
14	PORTD 1	-146	-749.5	28	PORTE 1	107	749.5
15	PORTD 2	-16	-749.5	-	-	-	-

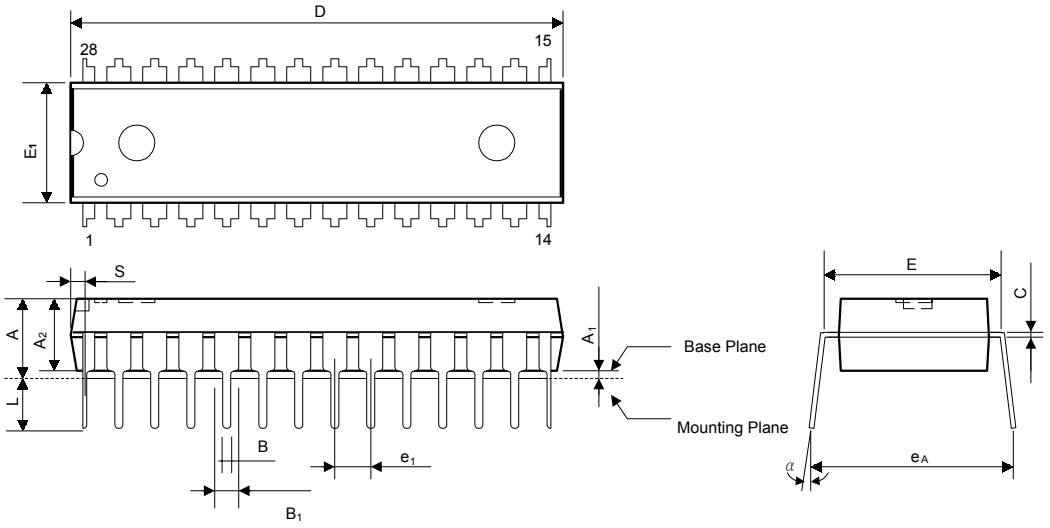
Ordering Information

Part No.	Packages
SH69P25H	CHIP FORM
SH69P25K	28L SKINNY
SH69P25M	28L SOP

Package Information

SKINNY_28L Outline Dimensions

unit: inches/mm

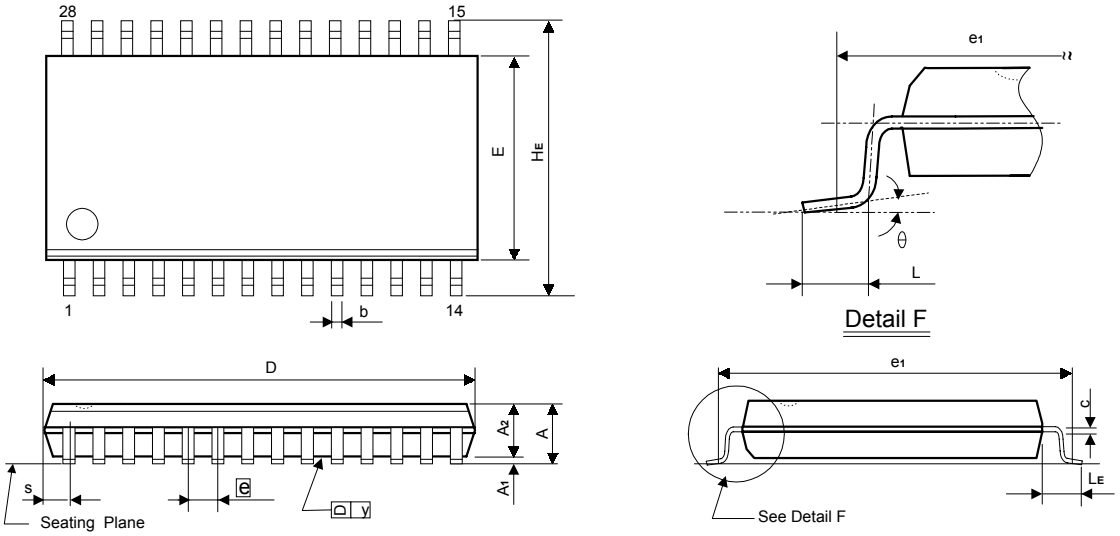


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.005	3.30 ± 0.13
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.388 Typ. (1.400 Max.)	35.26 Typ. (35.56 Max.)
E	0.310 ± 0.010	7.87 ± 0.25
E_1	0.288 ± 0.005	7.32 ± 0.13
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.350 ± 0.020	8.89 ± 0.51
S	0.055 Max.	1.40 Max.

Notes:

1. The maximum value of dimension D includes the end flash.
2. Dimension E_1 does not include the resin fins.
3. Dimension S includes the end flash.

SOP (N.B.) 28L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.093 ± 0.005	2.36 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.705 ± 0.020	17.91 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.40 NOM.
H_E	0.406 ± 0.012	10.31± 0.31
L	0.036 ± 0.008	0.91 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.043 Max.	1.09 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for the reference of PC Board surface mount pad pitch design only.
4. Dimension S includes end flash.

Data Sheet Version History

Version	Content	Date
0.2	Change Current limit Add “In System Programming Notice for OTP” Reduce operating current Add RC Frequency-Resistance diagram Add bonding diagram Change LVR low level voltage range from 2.5±0.1V to 2.5±0.2V	Nov. 2003
0.1	Original	Sep. 2002